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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,840	12/11/2003	Alex Chughen Chow	AUS920030713US1	2185

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Gregory W. Carr
670 Founders Square
900 Jackson Street
Dallas, TX 75202

EXAMINER

TRUONG, CAMQUY

ART UNIT	PAPER NUMBER
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2195

MAIL DATE	DELIVERY MODE
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01/15/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/733,840	Applicant(s) CHOW, ALEX CHUGHEN	
	Examiner Camquy Truong	Art Unit 2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 November 2007.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1- 2, 5-6, 9-10, 12-13, 15-16, and 19-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1- 2, 5-6, 9-10, 12-13, 15-16, and 19-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1- 2, 5-6, 9-10, 12-13, 15-16, and 19-20 are presented for examination.

Claims 3-4, 7-8, 11, 14, 17-18, 21-22 have been cancelled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-2, 5-6, 9-10, 12-13, 15-16, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sundaresan (U.S. Patent 6,289,369 B1) in view of Willen et al. (U.S. Patent 7,159,221 B1).

4. Sundaresan and Willen were cited in the last office action.

5. As to claim 1, Sundaresan teaches the invention substantially as claimed including: a method for load balancing in a tightly-coupled multiprocessor computer system comprising the steps of:

Dividing a task into a plurality of subtasks (the execution of a computer is divided into multiple threads, col. 1, lines 19-23);

placing the plurality of subtasks into a centralized task queue (Fig. 2; threads 22 resident in the central schedule queue 26, col. 5, lines 62-63);

distributing the plurality of subtasks in the centralized task queue to a plurality of library processors (threads 22 can migrate among processor 10, col. 5, lines 62-64; col. 8, lines 24-27);

wherein at least one subtask from the plurality of subtasks in the centralized task queue is distributed to at least one of the plurality of library processors when the library processor has at least one empty task buffer (if there is no eligible thread in the per-processor local queue, then the thread from the central queue is dispatched for execution, col. 8, lines 58-60); and

6. Sundaresan does not explicitly teach each library processor comprise exactly two task buffers; and one of the plurality of library processors fetching the subtask from the centralized task queue. However, Willen teaches each library processor comprise exactly two task buffers (each processor in the system has its own queues (SQ0 - SQn-1), col. 14, lines 56-57), and one of the plurality of library processors fetching the subtask from the centralized task queue (idle processor steal work from the queues of

processors that are busier on average, col. 11, lines 42-45; col. 15, lines 1-8; col. 16, lines 30-39).

7. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of each library processor comprise exactly two task buffers; and one of the plurality of library processors fetching the subtask from the centralized task queue as taught by Willen to the invention of Sundaresan because this allows to balance the system load while minimizing the overhead of fetching cached data from remote cache memories (col. 3, lines 12-14).

8. As to claim 2, Sundaresan teaches distributing the subtask from the plurality of subtasks in the centralized task queue to the one of the plurality of library processors when the one of the plurality of library processors has one or two empty task buffers (col. 8, lines 58-61).

9. As to claims 5-6, Willen teaches distributing the task from the plurality of subtasks in the centralized task queue to the one of the plurality of library processors by the one of the plurality of library processors fetching it from the centralized task queue when the load of the one of a plurality of library processors is zero or one subtasks (col. 2, lines 54-56; col. 16, lines 28-39; col. 19, lines 50-65; col. 23, lines 1-7).

10. As to claim 9, it is rejected for the same reason as claim 1. In addition, Willen

teaches a system kernel (Fig. 2; col. 5, lines 54-55).

11. As to claim 10, Sundaresan teaches each of the plurality of library processors is further configured to fetch a subtask from the library task queue when that library processor has at least one empty task buffer (col. 8, lines 58-61).

12. As to claims 12-13, Willen teaches the system kernel is comprised of a single processor and a plurality of processors (Fig. 2; col. 5, lines 49-53).

13. As to claim 15, it is rejected for the same reason as claim 1.

14. As to claim 16, it is rejected for the same reason as claim 2.

15. As to claims 19-20, it is rejected for the same reason as claims 5-6.

Response to the argument

16. Applicant arguments filed on 11/2/07 had been considered but they are not persuasive. In the remarks applicant argued (1) nowhere does Baumberger even hint that the one of the plurality of library processors has exactly two task buffers.

17. Examiner respectfully traverses Applicant's remarks: As to point (1), Willen teaches each processor in the system has its own queues (SQ0 - SQn-1), col. 14, lines

56-57) because Applicant has not disclosed that the exactly two task buffers provides an advantage, or solves a stated problem. Since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 and furthermore, discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to design a plurality of library processors wherein each processor has two task buffers.

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion


19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Camquy Truong whose telephone number is (571) 272-3773. The examiner can normally be reached on 8AM – 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3756.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIP. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIP system, contact the Electronic Business Center (EBC) at 866-217-9197(toll-free).

Camquy Truong

January 14, 2008


MENG-AL T. AN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100